

Introduction

Altera and Altera® Megafunction Partners Program (AMPPSM) partners offer a large selection of off-the-shelf megafunctions optimized for Altera devices. Designers can easily implement these parameterized blocks of intellectual property (IP), reducing design and test time. The OpenCoreTM feature allows users to evaluate Altera MegaCoreTM functions and AMPP megafunctions for free prior to licensing.

This document describes how to instantiate an AMPP or MegaCore function into a design and evaluate it using the OpenCore feature.

OpenCore Overview

Altera's exclusive OpenCore feature allows you to evaluate AMPP and MegaCore functions before deciding to license them. You can use the OpenCore feature to compile and simulate your design as well as verify the function's size and performance. However, the encrypted megafunction prevents you from generating a programming file. This evaluation provides first-hand functional, timing, and other technical data that helps you make an informed decision on whether to license the AMPP or MegaCore function. The OpenCore feature works a bit differently for AMPP and MegaCore functions:

- The AMPP partner provides a license file that activates the function through the OpenCore feature. The function is only available on a trial basis for a limited time.
- Altera MegaCore functions are available from the IP MegaStoreTM (<http://www.altera.com/IPmegastore>). You do not need a license file to use MegaCore functions with the OpenCore feature. Additionally, you can evaluate these functions for as long as you want.

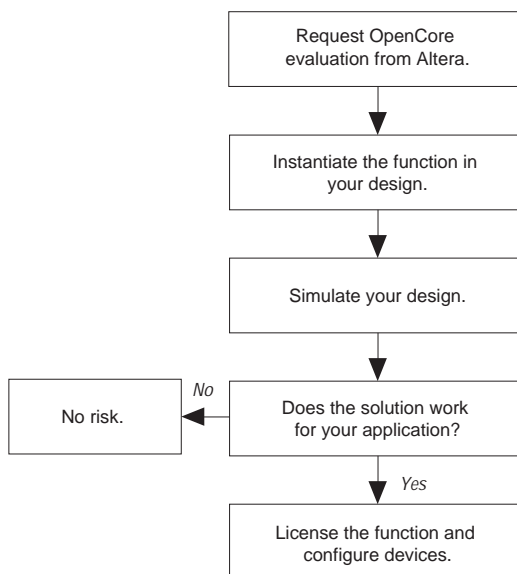
You cannot view the source code or retarget an AMPP or MegaCore function to a non-Altera device. Once you purchase a license for an AMPP or MegaCore function, you receive a license file from either the AMPP partner or Altera that lets you generate programming files and implement the megafunction on the device.



Designers working with the MAX+PLUS® II software must use version 9.1 or higher. Designers using the QuartusTM development system can use any version of the software.

Figure 1 shows a typical design flow using an AMPP or MegaCore function and the OpenCore feature.

Figure 1. OpenCore Evaluation Flow



MegaCore Functions

Altera develops and pre-tests MegaCore functions, optimizing them for specific Altera device architectures and allowing user-specified performance utilization goals to be met.

You can download MegaCore functions from the Altera web site (<http://www.altera.com>) by performing the following steps:

1. Go to the IP MegaStore web site (<http://www.altera.com/IPmegastore>).
2. Use the IP MegaSearch engine to find the function you want.
3. Click on the **Try** button for that function, and then click on the **Free Test Drive** button.
4. Complete and submit an Altera MegaCore License Agreement form.

5. Download the self-extracting compressed file for the megafunction you want. All the files necessary to instantiate the MegaCore function are included in this compressed file. Directions for downloading and uncompressing the self-extracting file on your PC or UNIX computer are included on the web site.

AMPP Functions

AMPP partners are third-party developers who provide a wide range of megafunctions optimized for Altera devices. AMPP partners also provide evaluation versions of their megafunctions. Use the following steps to request an evaluation megafunction from an AMPP partner:

1. Go to the IP MegaStore web site (<http://www.altera.com/IPmegastore>).
2. Use the IP MegaSearch engine to find the function you want.
3. Click on the **OpenCore** button on the function's web page in the IP MegaStore. Fill out the form and click **Send**.

Once the form is submitted, the AMPP partner emails the encrypted source files along with a license file that authorizes limited use of the function. You cannot view the source code or retarget an OpenCore function to a non-Altera device.

Symbol & Include Files

A Quartus Block Symbol File (**.bsf**) or a MAX+PLUS II Symbol File (**.sym**) and an Include File (**.inc**) are required to instantiate the OpenCore function into your Quartus or MAX+PLUS II design. These files are included with the function. A symbol file is necessary to instantiate a megafunction into a Quartus Block Design File (**.bdf**) or MAX+PLUS II Graphic Design File (**.gdf**). The Include File is used to instantiate a megafunction into a Text Design File (**.tdf**).



The MAX+PLUS II Compiler also uses Include Files to instantiate megafunctions in Verilog Design Files (**.v**). The megafunction is referenced in the Verilog Design File with a Module Instantiation. The Module Instantiation provides pin-out (i.e., name, width, and direction) and parameter information.



For more information on BSFs, Symbol Files, and Include Files, see Quartus or MAX+PLUS II Help.

Instantiating an OpenCore Function

This section outlines the procedures to instantiate an AMPP function into an existing graphical or textual (i.e., AHDL, VHDL, or Verilog HDL) design file. A graphical design requires a symbol file, and a textual or Verilog HDL design requires an Include File.



When evaluating a function with the OpenCore feature, you cannot simulate the function with a third-party simulator.

The following example describes how to instantiate the **encpt.vhd** megafunction into a Quartus BDF, MAX+PLUS II GDF, and TDF.

1. Request the function and license file on the Altera web site. After accepting your request, the AMPP partner will e-mail you the megafunction (**encpt.vhd**), license file (**encpt.dat**), BSF (**encpt.bsf**), Symbol file (**encpt.sym**), and Include file (**encpt.inc**).
2. Append the **FEATURE** line from the **encpt.dat** license file to the end of your existing Quartus or MAX+PLUS II license file. [Figure 2](#) shows a MAX+PLUS II license file with the encrypted **FEATURE** line.

Figure 2. MAX+PLUS II License File with encpt.vhd FEATURE Line

```

FEATURE maxplus2 alterad 2030.12 permanent uncounted CE0FE508668F \
HOSTID=GUARD_ID=T000031207
FEATURE quartus alterad 2030.12 permanent uncounted 8E74CEECE519 \
HOSTID=GUARD_ID=T000031207
FEATURE maxplus2verilog alterad 2030.12 permanent uncounted \
950CFD51E9C5 HOSTID=GUARD_ID=T000031207
FEATURE maxplus2vhd1 alterad 2030.12 permanent uncounted C250D62350FF \
HOSTID=GUARD_ID=T000031207
FEATURE C4D5_ABCD alterad 0000.00 03-dec-2000 uncounted AF008E1148CD \
VENDOR_STRING=i172A1A6MvN5d2o0qhWQAu$$ HOSTID=ANY
  
```

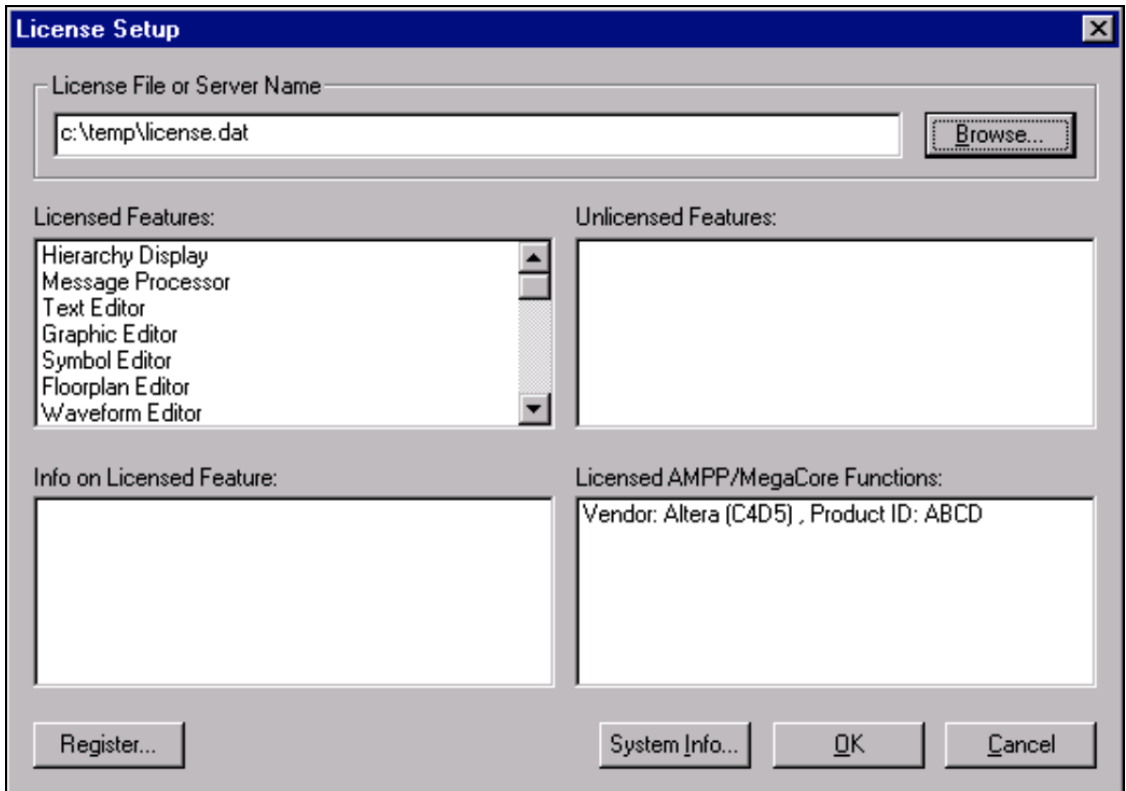
Once the **encpt.vhd** megafunction **FEATURE** line is appended to the license file, you can compile and simulate the function.



If your license file is on a server, restart the server so it will recognize the new **FEATURE** line in the license file.

3. To verify whether the function is licensed, choose **License Setup** (Options menu) in the MAX+PLUS II software (see [Figure 3](#)). The function should be listed in the **Licensed AMPP/MegaCore Functions** box. The Quartus software does not display which AMPP or MegaCore functions are licensed.

Figure 3. MAX+PLUS II License Setup Window

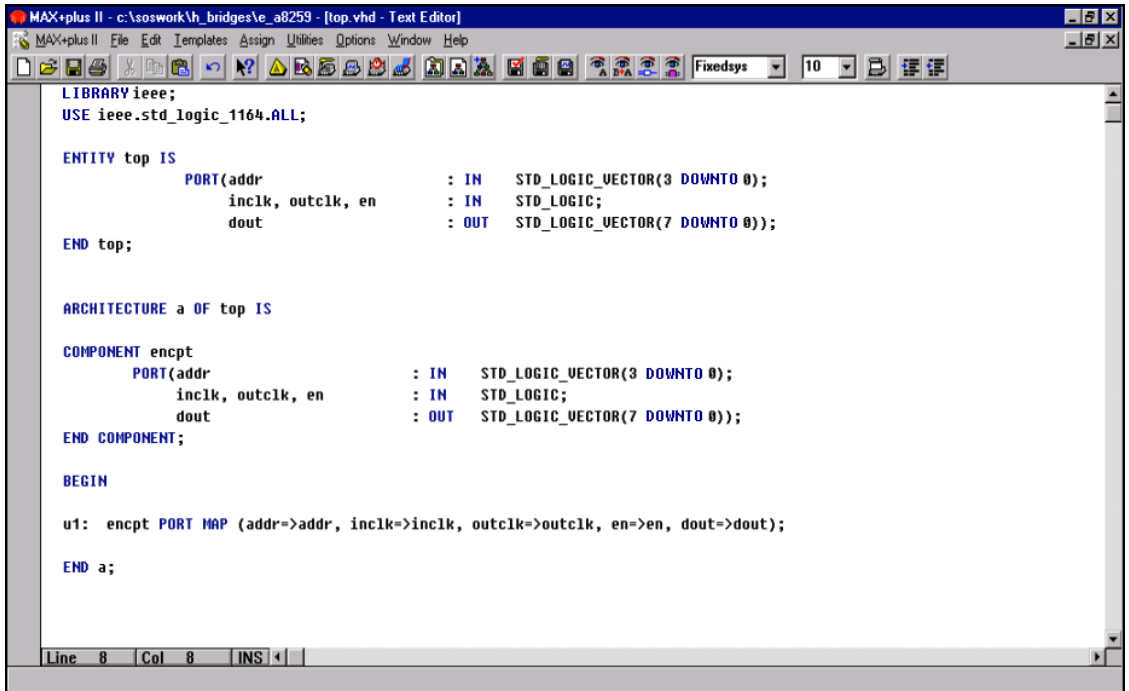


4. To instantiate **encpt.vhd**, open the BDF in the Quartus software or the GDF in the MAX+PLUS II Graphic Editor and designate a location within the design for the OpenCore megafunction. In the MAX+PLUS II Graphic Editor, select **Enter Symbol** (Symbol menu). In the **Enter Symbol** dialog box, select **encpt.sym**.
5. To instantiate **encpt.vhd** into a TDF, open the design in the Quartus or MAX+PLUS II Text Editor. Add the following line to the design:

```
INCLUDE "encpt.inc";
```

6. For VHDL designs, instantiate **encpt.vhd** with a Component Instantiation and then map to the megafunction within the design (see [Figure 4](#)).
7. Compile the design to verify its performance and utilization.

Figure 4. Instantiating *encpt.vhd* into a Top-Level VHDL File



```

LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY top IS
    PORT(addr          : IN  STD_LOGIC_VECTOR(3 DOWNTO 0);
          inclk, outclk, en : IN  STD_LOGIC;
          dout          : OUT STD_LOGIC_VECTOR(7 DOWNTO 0));
END top;

ARCHITECTURE a OF top IS

    COMPONENT encpt
        PORT(addr          : IN  STD_LOGIC_VECTOR(3 DOWNTO 0);
              inclk, outclk, en : IN  STD_LOGIC;
              dout          : OUT STD_LOGIC_VECTOR(7 DOWNTO 0));
    END COMPONENT;

    BEGIN

        u1: encpt PORT MAP (addr=>addr, inclk=>inclk, outclk=>outclk, en=>en, dout=>dout);

    END a;

```

Conclusion

The OpenCore feature allows you to evaluate MegaCore functions and AMPP megafunctions risk-free. You can use evaluation functions to instantiate, compile, and simulate a function to verify its size and performance before deciding to license it.



Notes:



101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
<http://www.altera.com>
[Applications Hotline:](#)
(800) 800-EPLD
[Customer Marketing:](#)
(408) 544-7104
[Literature Services:](#)
(888) 3-ALTERA

AHDL, Altera, AMPP, MAX+PLUS, MAX+PLUS II, MegaCore, OpenCore, and Quartus are trademarks and/or service marks of Altera Corporation in the United States and other countries. Altera acknowledges the trademarks of other organizations for their respective products or services mentioned in this document. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

Copyright © 2000 Altera Corporation. All rights reserved.

