



July 2000

Application Briefs

- AB 124 Prescaled Counters in FLEX 8000 Devices *Note (1)*
- AB 130 Parity Generators in FLEX 8000 Devices *Note (1)*
- AB 131 State Machine Encoding *Note (1)*
- AB 135 Ripple-Carry Gray Code Counters in FLEX 8000 Devices *Note (1)*

Application Notes

- AN 33 Configuring FLEX 8000 Devices *Note (1)*
- AN 36 Designing with FLEX 8000 Devices *Note (1)*
- AN 38 Configuring Multiple FLEX 8000 Devices *Note (1)*
- AN 39 IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices
- AN 41 PCI Bus Applications in Altera Devices
- AN 42 Metastability in Altera Devices
- AN 49 Implementing CRCCs in Altera Devices
- AN 51 Using Programmable Logic for Gate Array Designs
- AN 73 Implementing FIR Filters in FLEX Devices
- AN 74 Evaluating Power for Altera Devices
- AN 80 Selecting Sockets for Altera Devices
- AN 81 Reflow Soldering Guidelines for Surface-Mount Devices
- AN 82 Highly Optimized 2-D Convolvers in FLEX Devices
- AN 84 Implementing fft with On-Chip RAM in FLEX 10K Devices
- AN 86 Implementing the pci_a Master/Target in FLEX 10K Devices
- AN 88 Using the Jam Language for ISP & ICR via an Embedded Processor
- AN 91 Understanding FLEX 10K Timing
- AN 96 Performance Measurements of Typical Applications
- AN 97 Comparing Performance of High-Density PLDs
- AN 98 Comparing Performance of Common Megafunctions
- AN 99 Comparing Performance of Dual-Port Memory Functions
- AN 101 Improving Performance in FLEX 10K Devices with the Synplify Software

AN 102 Improving Performance in FLEX 10K Devices with Leonardo Spectrum Software
AN 106 Designing with 2.5-V Devices
AN 107 Using Altera Devices in Multiple Voltage Systems
AN 116 Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices

Brochures

Packaging Solutions Brochure

Catalogs

Intellectual Property Catalog
LPM Quick Reference Guide

Data Sheets

Altera Device Package Information Data Sheet
Altera Programming Hardware Data Sheet
BitBlaster Serial Download Cable Data Sheet
ByteBlaster Parallel Port Download Cable Data Sheet
ByteBlasterMV Parallel Port Download Cable Data Sheet
Configuration Elements Data Sheet
Configuration Devices for APEX & FLEX Devices Data Sheet
FLEX 10K Embedded Programmable Logic Family Data Sheet
FLEX 10KE Embedded Programmable Logic Family Data Sheet
FLEX 10K PCI Prototype Board Data Sheet
FLEX 10KE PCI Development Board Data Sheet
MasterBlaster Serial/USB Communications Data Sheet
Operating Requirements for Altera Devices Data Sheet
QFP Carrier & Development Socket Data Sheet

General Information

Introduction (to the Altera *1999 Data Book*)
Ordering Information

Product Information Bulletins

- PIB 20 Benefits of Embedded RAM in FLEX 10K Devices
- PIB 21 Implementing Logic with the Embedded Array in FLEX 10K Devices
- PIB 22 Design Tools for 100,000 Gate Programmable Logic Devices
- PIB 23 Digital Signal Processing in FLEX Devices

Selector Guides

Component Selector Guide

Technical Briefs

- TB 3 FLEX Devices as Alternatives to ASSPs & ASICs
- TB 4 Using FLEX Devices as DSP Coprocessors
- TB 5 Implementing Multipliers in FLEX 10K EABs
- TB 8 Implementing Multirate Filters in FLEX Devices
- TB 15 Implementing a 100,000-Gate Gate Array Design in an EPF10K100 Device
- TB 24 The Advantages of LPM
- TB 26 FLEX 10K & pci_a: The Complete PCI Solution
- TB 29 Internal Tri-State Emulation
- TB 31 The Advantages of FLEX 10K Devices Versus Lucent ORCA Devices
- TB 38 FLEX 10KA-1 Devices: The Fastest High-Density Devices Available
- TB 41 Power Measurements: FLEX 10KA vs. XC4000 Devices

Note:

- (1) Although this document was originally written for FLEX 8000 designs, it can also be used for FLEX 10K designs.