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Application Notes

- AN 39 IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices
- AN 42 Metastability in Altera Devices
- AN 74 Evaluating Power for Altera Devices
- AN 80 Selecting Sockets for Altera Devices
- AN 81 Reflow Soldering Guidelines for Surface-Mount Devices
- AN 85 In-System Programming Times for MAX Devices
- AN 88 Using the Jam Language for ISP & ICR via an Embedded Processor
- AN 95 In-System Programmability in MAX Devices
- AN 100 In-System Programmability Guidelines
- AN 107 Using Altera Devices in Multiple Voltage Systems

Brochures

Packaging Solutions Brochure

Catalogs

- AMPP Catalog
- LPM Quick Reference Guide

Data Sheets

- Altera Device Package Information Data Sheet
- Altera Programming Hardware Data Sheet
- BitBlaster Serial Download Cable Data Sheet
- ByteBlaster Parallel Port Download Cable Data Sheet
- ByteBlasterMV Parallel Port Download Cable Data Sheet
- Configuration Elements Data Sheet
- MasterBlaster Serial/USB Communications Data Sheet
- MAX 3000A Programmable Logic Device Family Data Sheet
- Operating Requirements for Altera Devices Data Sheet

General Information

Introduction (to the Altera *1999 Data Book*)

Ordering Information

Selector Guides

Component Selector Guide

Technical Briefs

TB 24 The Advantages of LPM

TB 28 Advantages of ISP-Based CPLDs

TB 32 ISP Programming Methods & Ordering Codes