Nios Soft Core Embedded Processor

June 2000, ver. 1 Data Sheet

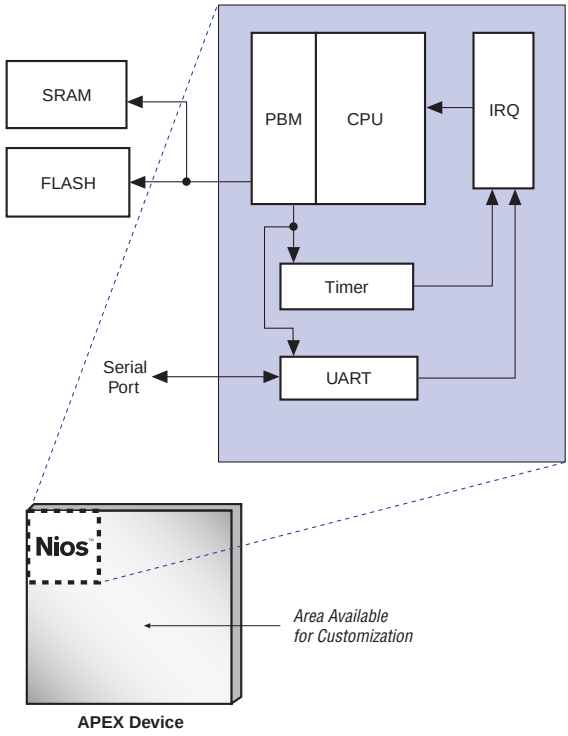
Features...

Part of Altera's Excalibur™ embedded processor solutions, the Nios™ soft core embedded processor is optimized for Altera® APEX™ programmable logic devices (PLDs) and system-on-a-programmable-chip (SOPC) integration. It is a general-purpose RISC processor core that is configurable to meet embedded design needs. Figure 1 shows the Nios embedded processor, which has the following features:

Preliminary Information

- Configurable load/store RISC architecture
  - Fully-synchronous address and data bus interface
  - Data path of 16 or 32 bits
    - 128 Kbyte and 8 Gbyte address range, respectively
  - 16-bit instruction set
    - Small memory footprint
    - Compatible with standard FLASH devices
  - Supports on-chip and off-chip memories
  - 5-stage pipeline architecture
    - One instruction per clock cycle
  - Windowed register access for fast interrupt handling
    - Up to 512 general-purpose registers
    - Window size: 32 registers
  - 64 vectored interrupts
- Customizable, on-chip peripherals
  - Universal asynchronous receiver/transmitter (UART), timer, parallel input/output (PIO), SRAM, and FLASH
  - Future peripherals include: serial peripheral interface (SPI), pulse-width modulation (PWM), IDE disk controller, 10/100 Ethernet controller media access controller (MAC), and an SDRAM controller
- Optimized for APEX programmable logic device (PLD) efficiency
  - Uses 13% of APEX EP20K200E device in 16-bit configuration
  - Uses 20% of APEX EP20K200E device in 32-bit configuration
  - Up to 50 MIPs and 50 MHz in an APEX EP20K200E device in 32-bit configuration
- Altera® MegaWizard® interface that configures the processor core, bus connections, and peripherals
  - Generates peripheral bus module (PBM)
  - Assigns IRQ numbers and priorities
  - Assigns peripheral base addresses
  - Implements 8-, 16-, and 32-bit data width configuration options (dynamic bus sizing)
  - Configures peripheral wait states

Figure 1. The Nios Embedded Processor



…and more Features

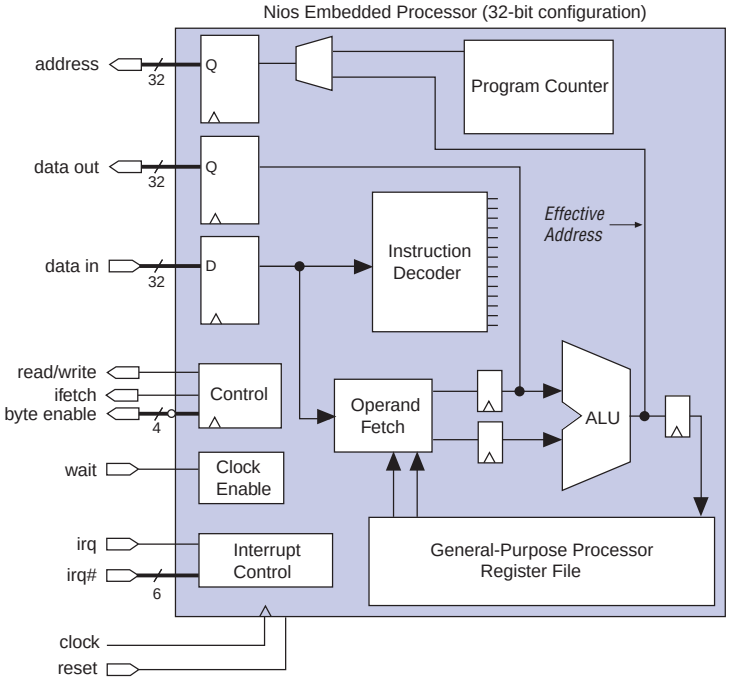
- Supported by GNUPro® industry-standard embedded system compile/debug tools created by Cygnus®, a Red Hat® company
  - C/C++ compiler
  - Assembler
  - Debugger
- The Excalibur Development Kit, featuring Nios
  - Nios development board, including an APEX EP20K200E device
  - Nios peripherals
  - MegaWizard interface
  - Quartus software
  - C/C++ compiler, debugger, and documentation
  - ByteBlaster download cable
  - Software drivers
  - SOPC reference design
  - User manual and programmer reference

For more information on the Excalibur Development Kit featuring Nios, refer to the *Excalibur Development Kit with the Nios Embedded Processor Data Sheet*.

General Description

The Nios embedded processor is a configurable, general-purpose RISC microprocessor that easily fits into an Altera® APEX™ device, leaving most of the logic available for peripherals and custom logic functions. The Nios embedded processor core is a pipelined, single-issue RISC processor in which instructions run in a single clock cycle. Figure 2 shows a block diagram of the Nios embedded processor.

Figure 2. Nios Embedded Processor Block Diagram *Note (1)*



Note:

(1) This diagram shows the 32-bit Nios configuration. In the 16-bit Nios configuration, the `address`, `data out`, and `data in` bus lines have 16 bits, and the `byte enable` bus line has 2 bits.

The Nios embedded processor core can be customized through a MegaWizard interface. Table 1 shows the Nios embedded processor core configuration options.

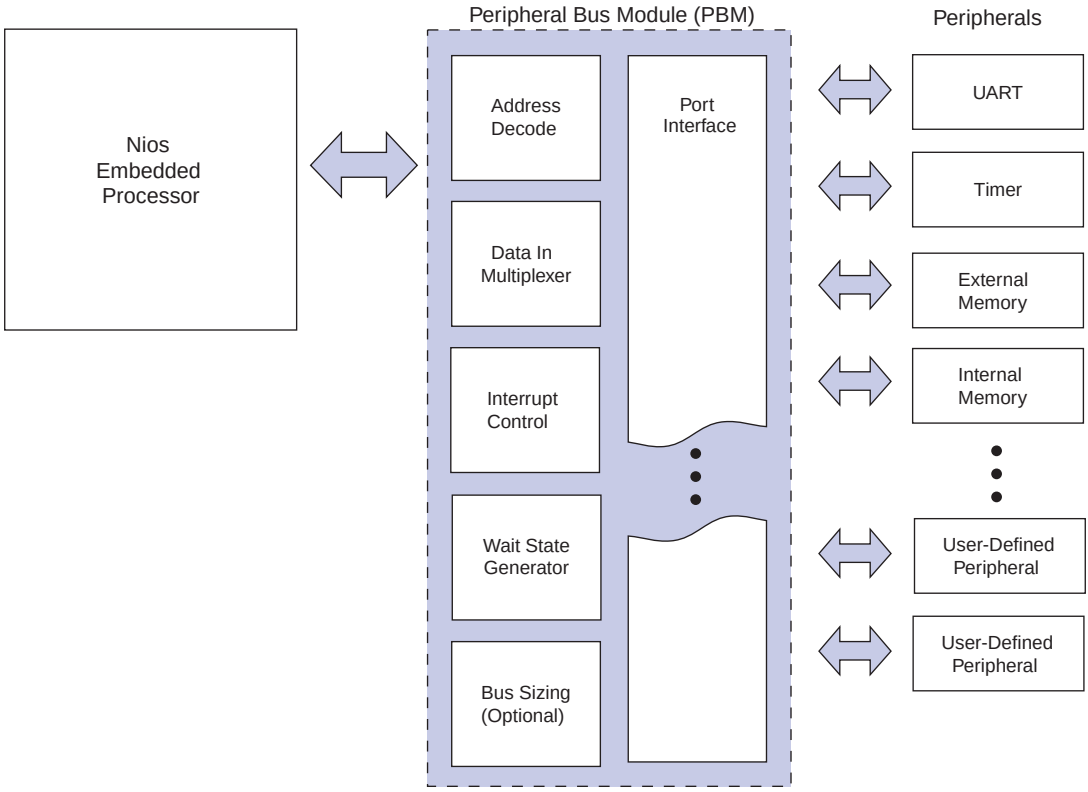
Table 1. Nios Embedded Processor Core Configuration Options

Feature	Comments
Data width	16 or 32 bits
Register file size	128 to 512 registers
Single clock shifts	1 to 31 bits

The MegaWizard interface allows the user to specify the embedded processor's connections to the rest of the system. Using a simple interface, the user can design an address map with different types, widths, and speeds of memory and peripherals. The MegaWizard interface generates the interface logic that connects all Nios peripherals as defined by the user.

Figure 3 diagrams the communication between the Nios embedded processor and user-defined peripherals.

Figure 3. Communication Between Nios Embedded Processor and Peripherals



As peripherals are added, the interface to each is specified. The MegaWizard Plug-In creates a peripheral bus module (PBM) according to the configuration specified.

The following PBM features are fully customizable:

- Base address
- Address span
- Data width
- Read-only/read-write/write-only
- Wait states
- IRQ signal/priority

The Nios embedded processor is supported by a full set of GNUPro embedded system development tools, created by Cygnus, a Red Hat company. These tools include a C/C++ compiler, assembler, and debugger.

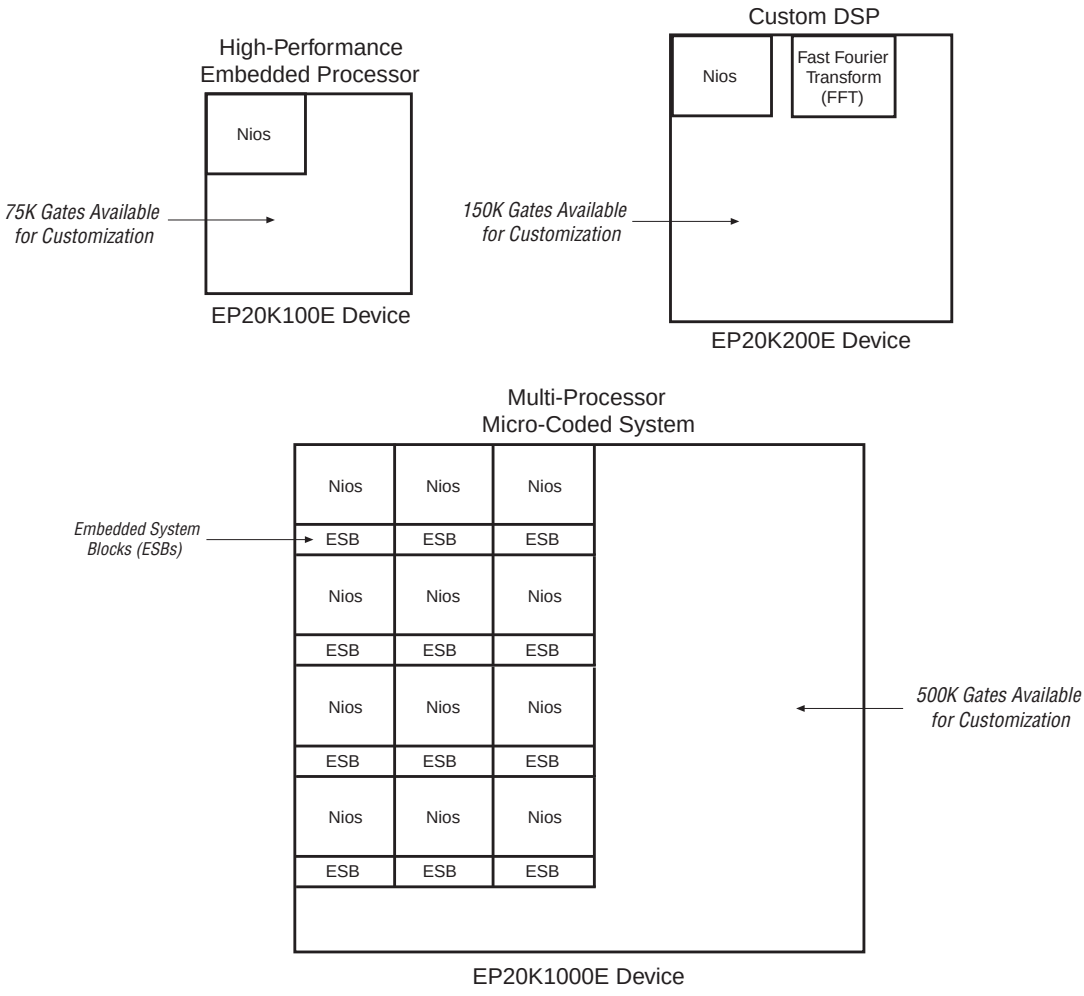
The Nios instruction set is targeted for compiled embedded applications and includes instructions that are especially useful in embedded systems (e.g., single-instruction bit-test-and-skip). The Nios core includes support for hardware breakpoints and run-control through the GNUPro debugger.

Typical Applications

The Nios embedded processor can be configured for a wide range of applications. A 16-bit implementation of the Nios core running a small program out of on-chip memory makes an effective sequencer/controller that may take the place of a hard-coded state machine. A 32-bit implementation of the Nios core with external FLASH program storage and large external main memory is a powerful 32-bit embedded processor.

Figure 4 gives an example of the flexibility and scalability of the Nios embedded processor.

Figure 4. Nios Flexibility and Scalability



A sample configuration of a 32-bit Nios embedded processor is shown below. Table 2 shows the sample configuration's device utilization specifications.

- 256 general-purpose registers
- One multiplier unit
- One UART (fixed baud rate)
- One 32-bit timer
- 512 bytes of on-chip ROM
- One 7-segment LED peripheral
- Peripheral bus module (PBM) (on-chip bus)
- SRAM interface (256 bytes)
- FLASH ROM interface (1 Mbyte)

Table 2. APEX Device Utilization

Device	Utilization Estimates				Data Path Configuration
	Logic Elements (LEs)	% of LEs	Embedded System Blocks (ESBs)	% of ESBs	
EP20K200E	1700	20	11	21	32-bit
	1100	13	7	13	16-bit
EP20K100E	1700	41	11	42	32-bit
	1100	26	7	27	16-bit

Conclusion

The Nios embedded processor provides a powerful and flexible solution for embedded systems developers. The combination of a configurable embedded processor, on-chip peripherals, and hardware and software development tools provides a complete solution for system-on-a-programmable-chip development.

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